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A SURVEY ON SIGMA DELTA MODULATION BASED ADC DESIGN

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ABSTRACT

Analog to digital conversion is one of the key challenges pertaining to digital communication systems. Although several analog to digital conversion schemes are at our disposal, yet most of them suffer from quantization noise and low accuracy. Sigma delta modulation is a technique that senses the noise effects in the digital signal and filters out the noise from the signal thereby rendering better accuracy and lesser noise effects in the recovered digital signal. This paper focuses on the basics of sigma delta modulation and provides insight into its working. It also provides the summary of the previous work done which paves the path for further research in system design.

Keywords: Sigma delta modulator, Over Sampling Rate, Signal to Noise Ratio, Dynamic Range, Quantization Noise

INTRODUCTION

Analog to Digital conversion plays a crucial role in all current day communication systems. In order to catch up with the current day technology advancements, sigma-delta converters are used with AN aim of high level of robustness and practicality with reduced chip price. it's applied in facility, medical devices, machine-driven production facilities, computers, weapons, navigation instrumentality, tools etc. Hence, if substantial analog signal process (ASP) is performed, random artifacts (noise) can accumulate, and also the ensuing signal might not represent the specified signal with the specified significance.[1] This paper focuses solely on delta-sigma modulation as chosen technique for A/D and D/A conversion. supported the mix of oversampling and quantization error shaping techniques Delta -sigma modulator deliver the goods a high degree of unfitness to analog circuit imperfections, so creating them a acceptable option to understand embedded analog-to-digital interfaces in trendy systems-on-chip (SoCs) integrated in millimicron CMOS.

Oversampling is inherently enforced in most sigma-delta (X-A) ADCs with integrated digital filters, wherever the modulator clock rate is often thirty two to 256 times the signal information measure, however X- A ADCs ar restricted for applications that need quick shift between input channels. In medical applications multiple devices face the hurdle of SNR e.g. myogram (EMG), cardiogram (ECG), so the paper focuses on medical devices that need higher SNR to enhance its performance.

High-performance data-acquisition signal chains utilized in medical instrumentality need wide dynamic vary and high accuracy. A delta-sigma device uses several samples from the modulator to provide a stream of 1-bit codes. The delta- letter of the alphabet ADC accomplishes this task by noise filtering. AN input- signal quantizer running at a high sample rate. The delta-sigma modulator takes AN input and produces a stream of digital values same as different quantizers that represents the voltage of the input. The delta-sigma modulators square measure of 2 varieties the time and therefore the frequency domain. A letter of the alphabet Delta Modulator contains a electric circuit, that is within the forward path of the loop. The modulator in Fig. 1 illustrates a primary order sigma-delta modulator. It contains of AN measuring system, a 1-bit quantizer, and a 1-bit DAC. The measuring system ramps the input signals up and down. The measuring system acts because the noise shaping circuit that shifts the noise from pass band to prevent band. The output of the measuring system is given to the comparator and so the comparator output is fed back through a 1-bit DAC to the Summing circuit. Oversampling is that the method of taking a lot of samples per second than needed on the premise of the Nyquist- applied scientist criterion. By everchanging the rate the signal power and total division noise power isn't affected. Therefore, the signal to division

noise magnitude relation isn't modified. However, the division noise is touch a bigger frequency varies, that reduces the spectral density of the division noise. The division noise power is reduced by three sound unit for each doubling of the oversampling magnitude relation and therefore the signal to division noise magnitude relation is improved consequently if the first Nyquist band is taken into account solely. The oversampling magnitude relation additionally affects the signal to noise magnitude relation. If oversampling is increased, the signal to noise magnitude relation is additionally increased exponentially.

PRINCIPLE OF OPERATION OF SIGMA DELTA MODULATORS

The following figure explains the principle of operation of sigma delta modulators.

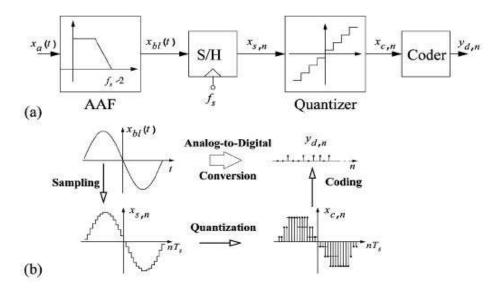


Fig.1 Block Diagram of a Sigma Delta Modulator

The sigma delta modulation process passes the original analog signal through an anti-aliasing filter to band-limit the signal. Then the sampling process is carried it using the sample and hold circuit. Further the quantization process is applied. Finally the encoding process ensues. It is worth mentioning that the next stage is a feedback filter in the loop that detects and removes the nose form the obtained digital signal.

PARAMETERS OF DELTA SIGMA MODULATION

(1) OVER SAMPLING RATIO:

When a significantly sampling frequency in a signal higher than the twice of bandwidth of digital samples known as Over sampling p, defined as

 $P = fs / 2B \tag{1}$

Where fs is the sampling frequency, B is the bandwidth or highest frequency of the signal, the nyquist rate is 2B.[2]

The theoretical limit of the SNR of Associate in Nursing ADC activity is predicated on the quantisation noise owing to the quantisation error inherent within the analog-to-digital conversion method once there's no oversampling and

averaging. Since the quantisation error depends on the quantity of bits of resolution of the ADC the simplest case SNR is calculated as a perform of the Effective range of Bits

SNR = (6.02 * ENOB) - 1.767 (2)

for the Effective number of bits, using the measured SNDR

ENOB = SNDR - 1.76 dB / 6.02 dB/bit (3)

Effective number of bits (ENOB) is simply the signal to noise-and-distortion ratio expressed in bits rather than decibels by solving the ideal SNR" equation [7] In the presentation of measured results, ENOB is identical to SNDR, with a change in the scaling of the vertical axis.

(2) QUANTIZATION AND QUANTIZATION ERROR

It is bound by [-A/2 to +A/2] where A represents the amplitude of the analog signal.

 $Qe_{(Max)} = \Delta/2$

Here Δ represents the step size.

(3) NOISE SHAPING:

The noise transfer function can be given by:

NTF (z) = $(1 - z^{-1}) L$ (4)

Where L denotes the order of filter

(4) DYNAMIC RANGE:

Dynamic range is the parameter exhibiting the variation of the signal in the time domain. It is mathematically given by:

$$A-(-A) = 2A \tag{5}$$

(5) FIGURE-OF-MERIT:

The figure of merit is the inverse of the signal to noise ratio and is given by

$$FOM = 1/SNR$$
(6)

Comparison of the power efficiency of two AD converters that achieve identical signal conversion specifications, i.e. have the same sampling rate and realize the same SNR for every input signal, is an easy task; the one with the lowest power consumption is the best. Although the FoM of combining weight, (6) is wide used, it cannot be accustomed build honest comparisons between low resolution and high resolution AD converters. once the resolution of associate ADC is inflated, some extent is reached wherever thermal noise is limiting the SNR, so as to scale back the impact of the noise by three sound unit, capacitances have to be compelled to be doubled to extend the amount of effective bits by one, a six sound unit reduction of the noise is needed, which implies an element four increase in capacitance. Since power scales linearly with the quantity of capacitance to charge, the facility will increase with an element four. Thus, the FoM can become a minimum of an element a pair of worse once the ENOB is inflated by one.

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PREVIOUS WORK

Jiandong Cheng et al. (2016) have suggested a new method for approximately calculating SNR of switched capacitor Sigma Delta Modulator. He suggested the truncation of NTF polynomial through Taylor's series with proper approximation which would provide the facility of fast calculation of SNR. For SNR calculation, the NTF is considered as rational function with the highest order of numerator and denominator should be same with equal coefficient. Through this method the sensitivity can also be measured with respect to the loop filter parameters.

Philip M. Choppet al. (2015) have proposed a frequency translating band pass Sigma Delta Modulator that down converts the 4 MHz bandwidth signal from 225MHz to 25 MHz. The bandpass SDM uses a single path mixing within the closed feedback loop which will simplify the synchronization of Local Oscillator (LO) frequency at the receiver end. The author has used 6th order loop filter, 3 bit quantizer and 100MHz as a sampling frequency. The bandpass noise shaping is performed around the 25MHz results in reduction of sensitivity of coefficient variation. This paper also concluded that the feedforward feedback loop filter technology is beneficial for improving the linearity, and reducing power consumption and the sensitivity to timing errors.

HisatoFujisakaet al. (2014) have proposed sorter based arithmetic circuits for Sigma Delta Domain Signal Processing. Fabricating circuits in nanometer - scale introduces electromagnetic interference and also transient device error which can cause system failure too. To overcome the above problem Pulse Signal Processing (PSP) is used i.e. Sigma Delta Domain Signal Processing (SDSP). For designing arithmetic and functional operations on SD modulated signal, sorting networks are used with two bit manipulation and permutation and for bit reversal NOT gate is used. Author has presented arithmetic modules like adder, exponential function. By using these modules, several transcendental functions and log- domain arithmetic operators can be designed.

Jose M. de la Rosa (2013) has described different design techniques of Sigma Delta Modulator. Fundamental of SDM contains the concept of oversampling and quantization. Sigma Delta Modulator also known as Noise shaping modulator as it pushes the noise out of band of interest and the Noise Transfer Function behaves as High Pass Filter or Band stop Filter. The Signal Transfer Function behaves as Low Pass Filter or Band Pass Filter allowing the low bandwidth baseband signals. The author also illustrated the effects of increase in order of modulator, OSR and quantizer bit. The author has also emphasized on the benefits of Sigma Delta Modulator as it provides high resolution, low power consumption, easy system - on -chip implementation in CMOS technologies, and can be used in number of application like digital receiver, Software defined Radio etc.

Philippe Benabeset al. (2011) have introduced high level system modeling for reducing the conception effort by using Fast Simulation techniques with MATLAB and VHDL AMS on Sigma Delta Modulator. In this work, design methodology for macro models extraction and high level modeling for continuous time functions was proposed for improvement of speed. A sixth order Sigma Delta Modulator is implemented from the extracted macro models which resulted in valid stable signal transfer function and improvement of simulation speed of about 30 times.

CONCLUSION

It can be concluded form the previous discussions that sigma delta modulation is an effective technique in analog to digital conversion and systems with specific design may yield less signal to noise ratios. Different structures though may yield slightly different values for the SDM parameters. This paper presents significant contributions in the related field that brings insight into the working of SDMs and further techniques to improve them.

REFERENCES

I. Yingqi Qian Changchun Zhang a, Zhongchao Liu, Leilei Liu, YurongLuan, Yuming Fang and Yufeng Guo, "A High-Performance Sigma-Delta Modulator in 0.18pm CMOS Technology" International Journal, Applied

Mechanics and Materials Vols. 519-520 (2014) pp 1085-1088, February 2014

- II. Fan Wenjie ,LvQiuye,HeChong,YinLiang,LiuXiaowei, "Architectural Design and Simulation of A Fourth-Order Sigma-Delta Modulator", International Journal, Key Engineering Materials Vols. 609-610 (2014) pp 723-727, April 2014
- III. Hetal Panchal, "Design and Simulation of Sigma Delta ADC Using VHDL AMS", International Journal of Engineering Development and Research, Volume 2, Issue 1, pp no.548-551, 2014
- IV. Liu Liang, Chen Song, He Chong, Yin Liang, Liu Xiaowei"Design of Third-order Single loop Full Feedforward Sigma Delta Modulator", International Journal, Key Engineering Materials Vols. 609-610 (2014) pp 1176-1180, April 2014
- V.RaminZanbaghi, Pavan Kumar Hanumolu "An 80-dB DR, 7.2-MHz Bandwidth Single OpampBiquad Based CT Modulator Dissipating 13.7-mW", IEEE Journal of Solid-State Circuits, Vol. 48, No. 2, pp 1 -15, February 2013
- VI. Jiandong Cheng, Guoyong Shi, and Ailin Zhang, "A Fast SNR Estimation Method for Sigma-Delta Modulator Design", TENCON 2013, IEEE Conference, 22nd -25th October ,pp 1-4, 2013
- VII. Philip M. Chopp and Anas A. Hamoui, "A 1-V 13-mWSingle-Path Frequency-Translating AZ Modulator With 55-dB SNDR and 4-MHz Bandwidth at 225 MHz", IEEE Journal of Solid-State Circuits, Vol. 48, No. 2, pp 1-14 February 2013
- VIII. HisatoFujisaka, Takeshi Kamio, Chang-Jun Ahn, Masahiro Sakamoto, and Kazuhisa Haeiwa "Sorter-Based Arithmetic Circuits for Sigma-Delta Domain Signal Processing—Part I: Addition, Approximate Transcendental Functions, and Log-Domain Operations", IEEE Transactions On Circuits and Systems—I: REGULAR PAPERS, Vol. 59, No. 9, ,pp no. 1952-1965, September 2012
 - IX. Jose M. de la Rosa, "Sigma Delta Modulators : Tutorial Overview, Design Guide, and State of the Art Survey ", IEEE Transaction on Circuits and System - I, Vol 58 No. 1, pp 121, January 2011
 - X. Philippe Benabes, Catalin-Adrian TUGUI, "Effective Modeling Of CT Functions For Fast Simulations Using MATLAB-Simulink And VHDL AMS applied to Sigma-delta Architectures" Circuits and Systems (ISCAS), IEEE Conference, Page No. 2269 - 2272, May 2011
- XI. Valeri Mladenov, "A Method for Validation the Limit Cycles of High Order Sigma-Delta Modulators", IEEE Conference, Nonlinear Dynamics and Synchronization (INDS) & 16th Int'l Symposium on Theoretical Electrical Engineering (ISTET), 2011 Joint 3rd Int'l Workshop, pp 1-5, 25-27 July 2011
- XII. JozefMihalov, VieraStopjakova, "Implementation of Sigma-delta Analog to Digital Converter in FPGA", IOP, Applied Electronics, IEEE Conference, Page No. 1-4, Sept. 2011
- XIII. Ahmed Shahein, Mohamed Afifi, Markus Becker, NiklasLotze, YiannosManoli, "A Power- Efficient Tunable Narrow-Band Digital Front End for Bandpass Sigma—Delta ADCs in Digital FM Receivers", Circuits and Systems II: Express Briefs, IEEE Conference, Vol. 57, Issue No. 11, pp 883 -887, November 2010
- XIV. Philippe Benabes, Ali Beydoun, Mohamad Javidan, "Frequency-band-decomposition Converters Using Continuous-time Sigma-Delta A/D Modulators", Circuits and Systems and TAISA Conference, IEEE Conference, Page No. 1-4, July 2009
- XV. Tao Wang and Liping Liang, "Analysis and Design of a Continuous-Time Sigma-Delta Modulator with 20MHz Signal Bandwidth, 53.6dB Dynamic Range and 51.4dB SNDR", 4 IEEE International Symposium on Electronic Design, Test and Applications, page no. 79-84, 2008
- XVI. Jesus Arias, Peter Kiss, Member, Vladimir Prodanov, Vito Boccuzzi, Mihai Banu, David Bisbal, Jacinto San Pablo, Luis Quintanilla and Juan Barbolla, "A 32-mW 320-MHz Continuous-Time Complex Delta-Sigma ADC for Multi-Mode Wireless-LAN Receivers", IEEE Journal of Solid-State Circuits, VOL. 41, NO. 2, pp no. 339 -351, February 2006
- XVII. Matthias Keller, Alexander Buhmann, Jens Sauerbrey, MauritsOrtmanns and YiannosManoli "A Comparative Study on Excess-Loop-Delay Compensation Techniques for
- XVIII. Continuous-Time Sigma—Delta Modulators'" IEEE Transactions on Circuits and Systems— I: Regular Papers, Vol. 55, No. 11,pp no.3480- 3487, December 2008
- XIX. J. Silva, U. Moon, J. Steensgaard and G.C. Temes" Wideband Low-distortion Delta-Sigma ADC Topology", Electronics Letters, IEEE Conference, Vol. 37, Issue : 12, Page No. 737 738, Jun 2001
- XX. Richard Schreier and Gabor C. Temes , " **Understanding Sigma Delta Data Converters**" ,IEEE Press, A John Wiley& Sons, Inc., Publication, Hoboken, NewJersey , 2005
- XXI. Steven R. Norsworthy, Richard Schreier and Gabor C. Temes" Delta Sigma Converters, Theory Design and Simulation" IEEE Press, IEEE Circuits and System Security, New York, 1997
- XXII. S.K. Mitra, "Digital Signal Processing- A Computer Based Approach", McGraw Hill, 3rd Edition, India, 2008

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